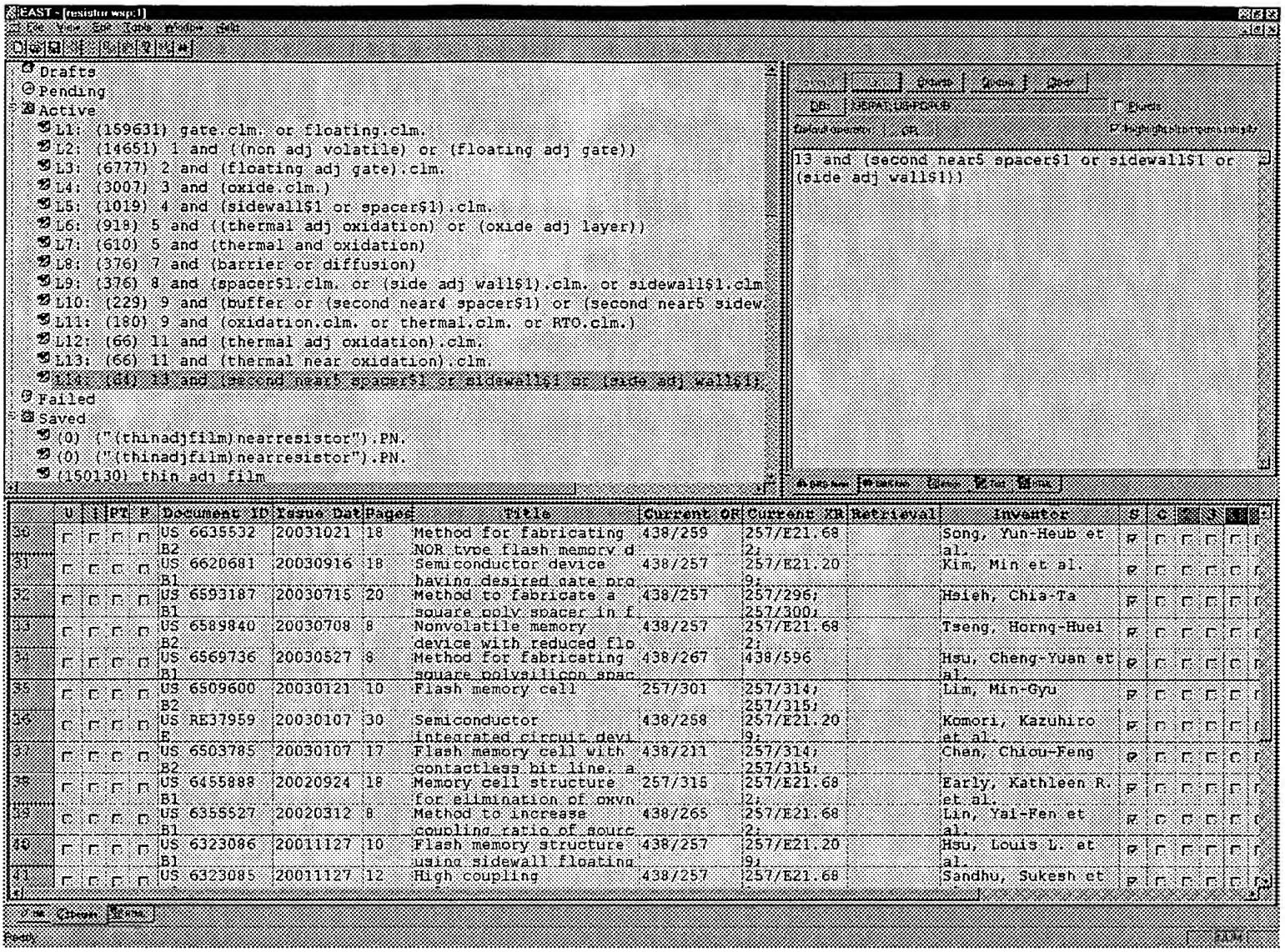
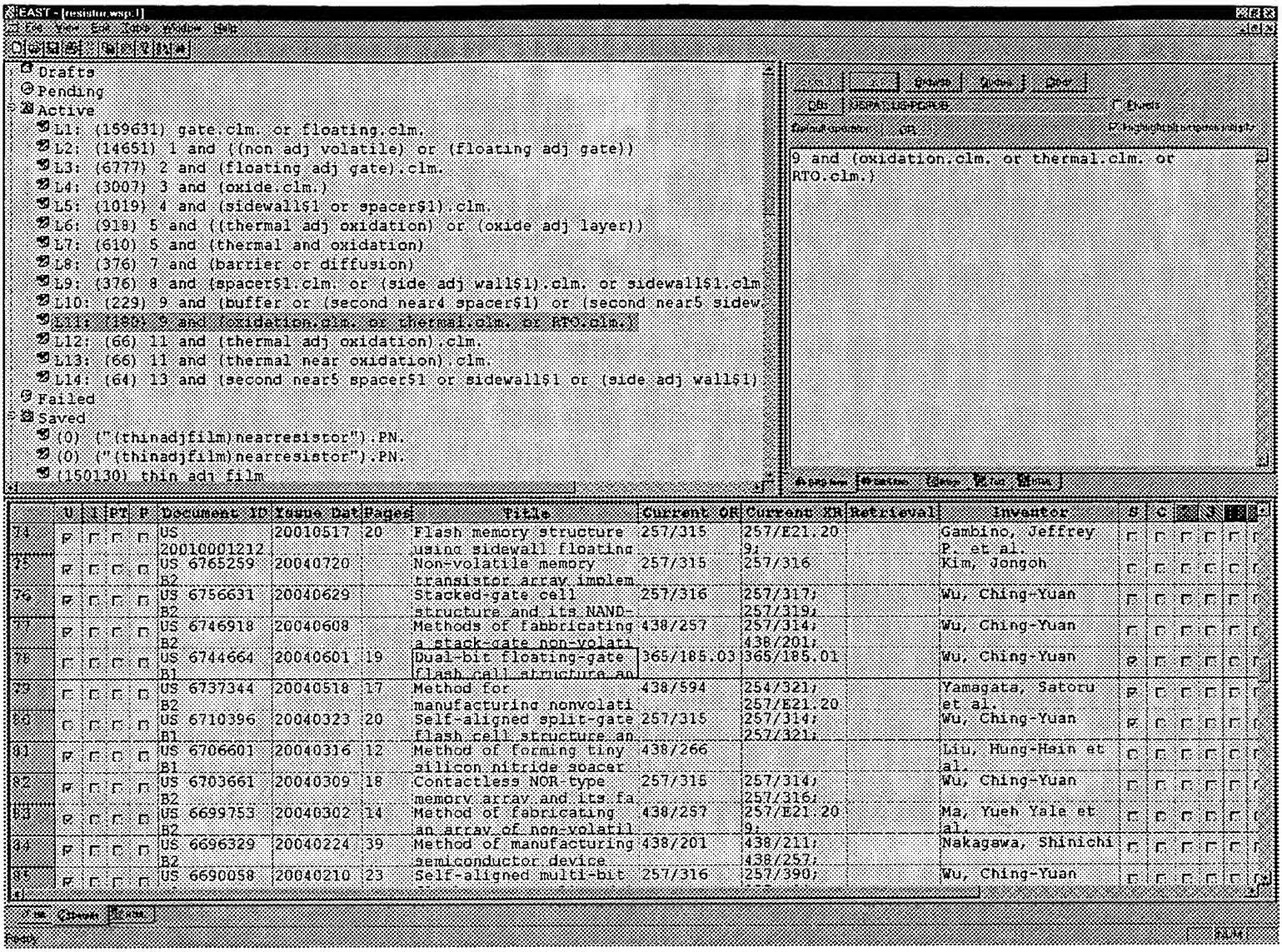


	U	I	PT	P	Document ID	Issue Dat	Pages	Title	Current OR	Current XR	Retrieval	Inventor	S	C
30					US 6635532 B2	20031021	18	Method for fabricating NOR type flash memory d	438/259	257/E21.68 2;		Song, Yun-Heub et al.	P	
31					US 6620681 B1	20030916	18	Semiconductor device having desired gate pro	438/257	257/E21.20 9;		Kim, Min et al.	P	
32					US 6593187 B1	20030715	20	Method to fabricate a square poly spacer in f	438/257	257/296; 257/300;		Hsieh, Chia-Ta	P	
33					US 6589840 B2	20030708	8	Nonvolatile memory device with reduced flo	438/257	257/E21.68 2;		Tseng, Horng-Huei	P	
34					US 6569736 B1	20030527	8	Method for fabricating square polysilicon spac	438/267	438/596		Hsu, Cheng-Yuan et al.	P	
35					US 6509600 B2	20030121	10	Flash memory cell	257/301	257/314; 257/315;		Lim, Min-Gyu	P	
36					US RE37959 E	20030107	30	Semiconductor integrated circuit devi	438/258	257/E21.20 9;		Komori, Kazuhiro et al.	P	
37					US 6503785 B2	20030107	17	Flash memory cell with contactless bit line, a	438/211	257/314; 257/315;		Chen, Chiou-Feng	P	
38					US 6455888 B1	20020924	18	Memory cell structure for elimination of oxyn	257/315	257/E21.68 2;		Early, Kathleen R. et al.	P	
39					US 6355527 B1	20020312	8	Method to increase coupling ratio of sourc	438/265	257/E21.68 2;		Lin, Yai-Fen et al.	P	
40					US 6323086 B1	20011127	10	Flash memory structure using sidewall floating	438/257	257/E21.20 9;		Hsu, Louis L. et al.	P	
41					US 6323085	20011127	12	High coupling	438/257	257/E21.68		Sandhu, Sukesh et	P	



	U	I	PT	P	Document ID	Issue Dat	Pages	Title	Current OR	Current XR	Retrieval	Inventor	S	C	2	3	4	5
74					US 20010001212	20010517	20	Flash memory structure using sidewall floating	257/315	257/E21.209;		Gambino, Jeffrey P. et al.						
75					US 6765259 B2	20040720		Non-volatile memory transistor array implem	257/315	257/316		Kim, Jongoh						
76					US 6756631 B2	20040629		Stacked-gate cell structure and its NAND-	257/316	257/317; 257/319;		Wu, Ching-Yuan						
77					US 6746918 B2	20040608		Methods of fabbricating a stack-gate non-volati	438/257	257/314; 438/201;		Wu, Ching-Yuan						
78					US 6744664 B1	20040601	19	Dual-bit floating-gate flash cell structure an	365/185.03	365/185.01		Wu, Ching-Yuan						
79					US 6737344 B2	20040518	17	Method for manufacturing nonvolati	438/594	254/321; 257/E21.20		Yamagata, Satoru et al.						
80					US 6710396 B1	20040323	20	Self-aligned split-gate flash cell structure an	257/315	257/314; 257/321;		Wu, Ching-Yuan						
81					US 6706601 B1	20040316	12	Method of forming tiny silicon nitride spacer	438/266			Liu, Hung-Hsin et al.						
82					US 6703661 B2	20040309	18	Contactless NOR-type memory array and its fa	257/315	257/314; 257/316;		Wu, Ching-Yuan						
83					US 6699753 B2	20040302	14	Method of fabricating an array of non-volatil	438/257	257/E21.209;		Ma, Yueh Yale et al.						
84					US 6696329 B2	20040224	39	Method of manufacturing semiconductor device	438/201	438/211; 438/257;		Nakagawa, Shinichi						
85					US 6690058	20040210	23	Self-aligned multi-bit	257/316	257/390;		Wu, Ching-Yuan						

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